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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,722	06/13/2005	Arild Wego	P17026US1	7297

27045 7590 03/17/2008

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EXAMINER	
NGUYEN, MINH TRANG T	

ART UNIT	PAPER NUMBER
4134	

MAIL DATE	DELIVERY MODE
03/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,722	WEGO ET AL.	
	Examiner	Art Unit	
	MINH-TRANG NGUYEN	4134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/22/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 9* is/are rejected.

7)☒ Claim(s) *3-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/13/2005, 12/22/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "the circuit switched node" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 1, 2 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Petty et al. [5,862,131] in view of Carney et al. [5,940,384].

As to **claim 1**, Petty et al. disclose an arrangement for interconnection of two or more printed circuit boards communicating with each other over a time division multiplex data bus, each including a number of loads transferring data in both receive and transmit direction (see Figs. 1 and 2, col. 7 lines 15-30), comprising: a local time division multiplex data bus in each printed circuit board to which the associated number of loads are connected (see Fig 2, MUX A + B 212; col. 3, line 51 to col. 4, line 12); an intermediate central processing unit controlled logic (see Fig 2, items 108, 203, col. 4, lines 36-41) in each direction connecting each local time division multiplex data bus (see Fig. 2, MUX A + B 212) to a global time division multiplex data bus (Fig. 2, item 105, col. 3, lines 51-65), which logic includes a buffer (see Fig. 2, items 200, 201, 205, 207, col. 3, line 51 to col.4 line 9) through which synchronous data from the respective local time division multiplex data bus or the global time division multiplex data bus is being written in and read out to the respective local time division multiplex data bus or the global time division multiplex data bus introducing a phase difference providing a total delay for any data traveling from the respective local time division multiplex data bus to the global time division multiplex data bus and back to the respective local time division multiplex data bus being of a controllable dimension equal to an integer number of data frames (see col. 3, line 65 - col. 4, line 44, e.g., the phase difference between

TDM clock 213 and Frame clock 214 provides total delay equal to an integer number of data frames).

Petty et al. do not expressly disclose that the buffer is a FIFO buffer.

Carney et al. disclose that it is known in the art to use a FIFO buffer for storing data received/transmitted from a TDM data bus (see Fig. 5, item 210, col. 10, lines 22-28 ; Fig. 6, item 214, col. 10, lines 38-40).

Petty et al. and Carney et al. are analogous art because they relate to controlling TDM data bus.

At the time of invention, it would have been obvious to a person of ordinary skilled in the art to use the FIFO buffer taught by Carney et al. in Petty et al's buffer. The suggestion/motivation would have been maintaining the order to the data as it is process, the exact function of a FIFO.

As to **claim 2**, Petty et al. disclose that the global time division multiplex data bus is a back plane time division multiplex data bus, and said arrangement is implemented in a circuit switched node (col. 1, lines 64-65; col. 2, lines 1-15).

As to **claim 9**, Petty et al. disclose that the circuit switched node is a switch in any circuit switched enabled data or telecommunication network (see Fig. 1, col. 1 lines 8-30).

Allowable Subject Matter

6. **Claims 3-8** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: None of the prior art teaches that "the logic further includes a first and a second time slot counter, the first counter addressing a first data location in the First-In-First-Out buffer into which, in case of receive direction, time slot data from a local time division multiplex data bus is to be written, or out of which, in case of transmit direction, time slot data to a local time division multiplex bus is to be read, the second counter addressing a second data location in the First-In-First-Out buffer into which, in case of transmit direction, time slot data from the global time division multiplex bus is to be written, or out of which, in case of receive direction, time slot data to the global time division multiplex bus is to be read, wherein the phase difference between the first and the second time slot counter represents a preferred part of said total delay caused by the logic of the respective direction" as recited in claim 3.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patton [6,393,020] and Williams [6,370,386] disclose the multiple local simple communication buses are connected as part of a lager global communication bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MINH-TRANG NGUYEN whose telephone number is (571)270-5248. The examiner can normally be reached on Monday to Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lun-Yi Lao can be reached on 571-272-7671. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MINH-TRANG NGUYEN/
Examiner, Art Unit 4134

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Examiner, Art Unit 4134*

/LUN-YI LAO/

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